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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 June 2006</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-17,20-34,36-38,41-43,45 and 46* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-17,20-34,36-38,41-43,45 and 46* is/are rejected.

7)☐ Claim(s) _____ , is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new grounds of rejection.

2.   Applicant's arguments filed June 8, 2006, with respect to the rejection of claims 34 and 36-38 under 35 USC 102 have been fully considered but they are not persuasive. The Examiner respectfully disagrees with the Applicant's arguments on pages 13 and 14 of the Remarks that Moshayedi fails to disclose counting down of a counter. The previous Office Action included a definition of "increment" in which a negative change was included. Further, regardless of whether a counter is counting up or down, the prior art reference Moshayedi is interpreted as disclosing an equivalent means and end as that recited in Applicant's invention as claimed. Therefore, the Applicant's invention as claimed is not warranted patentable in view of Moshayedi (please see MPEP 2184(II)(A)).

3.   Applicant's arguments, see page 14 of the Remarks, filed June 8, 2006, with respect to the rejection of claims 45 and 46 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Moshayedi and Official Notice.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 20 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Claim 20 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 20 discloses a memory system of a SmartMedia card which independent claim 6 discloses the "memory system" as comprising "a controller". The Applicant's Specification on page 16 in lines 25-27 states that a SmartMedia card does not include a controller.

Claim 21, of which claim 30 is ultimately dependent upon, discloses in line 3 the limitation "a memory system on a first chip". Claim 30 discloses a memory card, which is defined in claim 29 as "the memory system", as being selected from a group comprising various memory cards. The Examiner interprets a memory "card" as not being able to be "on" a "chip", but rather a memory "card" itself is comprised of one or more "chips".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 6-7, 9-14, 16-17, 34, 36-38, and 41-43 are rejected under 35 U.S.C. 102(e) as

being anticipated by Moshayedi (U.S. PGPub 2002/0091965).

As in claim 6, Moshayedi discloses a memory system for storing information, the

memory system comprising:

a first plurality of spare units of erase on a first chip *(Fig. 2; paragraphs [0038]-[0040]*

and [0048]; paragraphs [0034], [0037], [0038], and [0048] disclose a plurality of memory

chips which contain spare units of erase);

a second plurality of spare units of erase on a second chip *(Fig. 2; paragraphs [0041]-*

[0042] and [0048]; paragraphs [0034], [0037], [0038], and [0048] disclose a plurality of

memory chips which contain spare units of erase);

a first storage element on the first chip, the first storage element containing a first counter

and a first threshold *(paragraphs [0050] and [0053])*, the first counter indicating a number of

spare units of erase on the first chip which have not yet been reassigned *(paragraphs [0050] and*

[0053]);

a second storage element on the second chip, the second storage element containing a

second counter and a second threshold *(paragraphs [0050] and [0053])*, the second counter

indicating a number of spare units of erase on the second chip which have not yet been

reassigned *(paragraphs [0050] and [0053]; paragraphs [0034], [0037], [0038], and [0048]*

disclose a plurality of memory chips which contain spare units of erase);

a controller, the controller updating the first counter each time a spare unit of erase of the

first plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*,

the controller comparing the first counter to the first threshold value, the controller updating the

second counter each time a spare unit of erase of the second plurality of spare units of erase is

reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, the controller comparing the second

counter to the second threshold value, the controller generating an end-of-life indicator when

either the first counter reaches the first threshold or the second counter reaches the second

threshold *(paragraphs [0048] and [0056], where it is interpreted that because there are multiple*

chips that may fail and that have respective spare locations, the controller will treat both a first

chip and a second chip in the same manner when determining if a chip exhibits a failure

condition); and

wherein the memory system operates in conjunction with a host system *(Figs. 1A and 1B;*

paragraphs [0032]-[0037]) and the controller reassigns a spare unit of erase in response to a

request from the host system *(paragraphs [0032]-[0036])*.

As in claim 7, Moshayedi discloses the controller compares the first counter to the first threshold value to determine if the memory system is in an end-of-life condition, the controller determines that the memory system is in the end-of-life condition when a value of the first counter is less than or equal to the first threshold value *(Abstract, paragraph [0053])*.

As in claim 9, Moshayedi discloses the controller attempts to write data to a first unit of erase on the first chip, and determines if the first unit of erase is worn *(paragraphs [0041]- [0043])*.

As in claim 10, Moshayedi discloses when it is determined the first unit of erase is worn, the controller reassigns a first spare unit of erase included in the first plurality of spare units of erase as the first unit of erase *(paragraphs [0041]-[0043])*.

As in claim 11, Moshayedi discloses the controller writes the data into the reassigned first spare unit of erase *(paragraphs [0041]-[0043])*.

As in claim 12, Moshayedi discloses the controller is still further arranged to attempt to write data to a first unit of erase on the first chip to determine if the first unit of erase is defective *(paragraphs [0040]-[0043])*.

As in claim 13, Moshayedi discloses when it is determined that the first unit of erase is defective, the controller reassigns a first spare unit of erase included in the first plurality of spare units of erase as the first unit of erase *(paragraphs [0040]-[0043])*.

As in claim 14, Moshayedi discloses the controller writes the data into the reassigned first spare unit of erase *(paragraphs [0040]-[0043])*.

As in claim 16, Moshayedi discloses a non-volatile memory, wherein the first plurality of spare units of erase, the second plurality of spare units of erase, and the first storage element are included in the non-volatile memory *(paragraphs [0007] and [0034])*.

As in claim 17, Moshayedi discloses the memory system is a non-volatile memory system *(paragraphs [0007] and [0034])*.

As in claim 34, Moshayedi discloses a memory system for storing information, the memory system comprising:

a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*;

means for storing a counter *(paragraphs [0036] and [0050])*;

means for storing a threshold *(paragraphs [0036] and [0053])*;

means for reassigning a spare unit of erase of the plurality of spare units of erase *(paragraphs [0041]-[0043])*;

means for decrementing the counter *(Abstract, paragraphs [0016] and [0050], page 7 claim 36)*, the counter being arranged to be decremented each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050])*;

means for comparing the counter to the threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are yet to be reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-[0055])*; and

means for generating an indication when comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is substantially near a failure condition *(paragraphs [0053]-[0055])*.

As in claim 36, Moshayedi discloses the means for comparing the counter to the threshold value include means for determining when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 37, Moshayedi discloses the first result is arranged to indicate that the value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0056])*.

As in claim 38, Moshayedi discloses means for attempting to write data to a first unit of erase *(paragraphs [0040]-[0042])*;

means for determining when the first unit of erase is worn, wherein the means for

reassigning the unit of erase include means for reassigning a first spare unit of erase included in

the plurality of spare units of erase as the first unit of erase when it is determined that the first

unit of erase is worn *(paragraphs [0041]-[0043])*, and wherein the means for updating the

counter include means for updating the counter to indicate that the first spare unit of erase is

reassigned *(paragraph [0050], page 7 claim 36)*; and

means for writing the data to the reassigned first spare unit of erase *(paragraph [0042])*.

As in claim 41, Moshayedi discloses a method for determining a status associated with a

non-volatile memory system *(paragraphs [0007] and [0034])*, the non-volatile memory system

including a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*, the

method comprising:

automatically determining when the non-volatile memory system is nearing a condition

which renders the non-volatile memory system as being substantially unreliable *(paragraphs

[0053]-[0055])*;

generating an indication when it is determined that the non-volatile system is nearing the

condition which renders the non-volatile memory system as being substantially unreliable

(Abstract, paragraph [0056], page 7 claim 35), wherein the indication is arranged to indicate

that the non-volatile memory system is nearing the condition which renders the non-volatile

memory system as being substantially unreliable *(paragraphs [0053]-[0056])*;

saving the indication *(paragraph [0056], where the indication is the updating of

information)*;

wherein automatically determining when the non-volatile memory system is nearing a

condition which renders the non-volatile memory system as being substantially unreliable

includes:

updating a counter, the counter being arranged to be updated each time a spare unit of

erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7*

claim 36), wherein the counter indicates a number of spare units of erase remaining in the

plurality of spare units of erase *(paragraph [0050])*; and

comparing the counter to a threshold value, the threshold value being indicative of a

number of spare units of erase of the plurality of spare units of erase which are not to be

reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-*

[0055]).

As in claim 42, Moshayedi discloses generating the indication when it is determined the

non-volatile system is nearing the condition which renders the non-volatile memory system as

being substantially unreliable includes:

determining when comparing the counter to the threshold value yields a first result,

wherein the indication is arranged to indicate that the memory system is nearing the condition

which renders the non-volatile memory systems as being substantially unreliable when

comparing the counter to the threshold value yields the first result *(paragraphs [0053]-[0055])*.

As in claim 43, Moshayedi discloses the condition which renders the non-volatile

memory systems as being substantially unreliable when comparing the counter to the threshold

value yields the first result is one of an end-of-life condition and a fault condition *(Abstract, paragraphs [0053]-[0056])*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1-5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Auclair et al. (U.S. Patent No. 6,016,530).

As in claim 1, Moshayedi teaches a method for determining a status associated with a memory system, the memory system including a plurality of spare units of erase, the method comprising:

receiving user data for storage in the memory system *(paragraph [0035])*;

storing the user data in a first unit of erase if the first unit of erase is not unreliable *(paragraph [0040])*;

reassigning a first spare unit of erase of the plurality of spare units of erase in the reassigned first spare unit of erase if the first unit of erase is unreliable *(paragraphs [0041]- [0042])*;

updating a counter each time a spare unit of erase of the plurality of spare units of erase is

reassigned *(page 7 claim 36)*, wherein the counter indicates a number of spare units of erase

remaining in the plurality of spare units of erase *(paragraph [0050] lines 7-9, page 7 claims 35*

and 36);

comparing the counter to a threshold value, the threshold value being indicative of a

number of spare units of erase of the plurality of spare units of erase which are yet to be

reassigned in order for the memory system to be considered as reliable *(paragraphs [0053]-*

[0054], page 7 claim 35); and

generating an indication when comparing the counter to the threshold value yields a first

result, wherein the indication is arranged to indicate that the memory system is substantially near

a failure condition *(Abstract, paragraph [0056], page 7 claim 35, where an action taken is*

interpreted as a first result).

However, Moshayedi fails to teach of error correction codes. Auclair et al. teaches of

calculating an error correction code from the user data and storing the error correction code

together with the user data in units of erase *(column 7 lines 18-22)*.

It would have been obvious to have included the error correction codes as taught by

Auclair et al. in the invention of Moshayedi. This would have been obvious because the

invention of Auclair et al. offers a fault tolerant fast-access, low power memory storage *(column*

1 lines 34-60). Further, it is well-known in the art to include ECC data in conjunction with user

data for fault tolerance when saving such data to a memory device.

As in claim 2, Moshayedi discloses updating the counter includes decrementing the counter each time a spare unit of erase of the plurality of spare units of erase is reassigned *(Abstract, paragraph [0016], page 7 claim 36)*.

As in claim 3, Moshayedi discloses comparing the counter to the threshold value includes determining when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 4, Moshayedi discloses the first result is arranged to indicate that the value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0056])*.

As in claim 5, Moshayedi discloses attempting to write data to a first unit of erase *(paragraphs [0040]-[0042])*;

determining when the first unit of erase is worn *(paragraphs [0041]-[0042])*;

reassigning a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase when it is determined that the first unit of erase is worn *(paragraphs [0041]-[0043])*, wherein updating the counter includes updating the counter to indicate that the first spare unit of erase is reassigned *(paragraph [0050], page 7 claim 36)*; and

writing the data to the reassigned first spare unit of erase *(paragraph [0042])*.

As in claim 15, Moshayedi teaches an individual one of the first plurality of spare units of erase is a memory location, and an individual one of the second plurality of spare units of erase

is a spare memory location *(Fig. 2; paragraph [0039])*. However, Moshayedi fails to explicitly

state that the memory location is a sector. Auclair et al. teaches of a flash memory location as

being a sector *(Abstract, column 2 lines 18-24)*.

It would have been obvious to have included the sectors as taught by Auclair et al. in the

invention of Moshayedi. This would have been obvious because the invention of Auclair et al.

offers a fault tolerant fast-access, low power memory storage *(column 1 lines 34-60)*. Further, it

is well-known in the art to allocate flash memory sections as sectors.

*   *   *

7.   Claims 20, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Moshayedi in view of Official Notice.

As in claim 20, Moshayedi teaches the limitations of claim 6. However, Moshayedi fails

to teach the non-volatile memory is one of a PC card, a CompactFlash card, a MultiMedia card, a

Smart Media card, a Memory Stick card, and a Secure Digital card *(paragraphs [0007] and

[0034])*. The Examiner takes Official Notice that one of ordinary skill in the art would have

thought it obvious to have implemented any one of the above-mentioned types of memory cards

in the invention of Moshayedi. This would have been obvious because the above-mentioned

memory cards are well-known in the art.

As in claim 45, Moshayedi teaches a non-volatile memory system for storing information *(paragraphs [0007] and [0034])*, the non-volatile memory system comprising:

a plurality of spare units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*;

means for automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0055])*; and

means for generating an indication when it is determined that the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(Abstract, paragraph [0056], page 7 claim 35)*, wherein the indication is arranged to indicate that the non-volatile memory system is nearing the condition which renders the non-volatile memory system as being substantially unreliable *(paragraphs [0053]-[0056])*;

wherein the non-volatile memory is one of a memory card *(paragraphs [0007] and [0034])*;

wherein the means for automatically determining when the non-volatile memory system is nearing a condition which renders the non-volatile memory system as being substantially unreliable include:

means for updating a counter, the counter being arranged to be updated each time a spare unit of erase of the plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*, wherein the counter indicates a number of spare units of erase remaining in the plurality of spare units of erase *(paragraph [0050])*; and

comparing the counter to a threshold value, the threshold value being indicative of a number of spare units of erase of the plurality of spare units of erase which are not to be

reassigned in order for the memory system to be considered as useable *(paragraphs [0053]-[0055])*.

However, Moshayedi fails to teach the non-volatile memory is one of a PC card, a CompactFlash card, a MultiMedia card, a Smart Media card, a Memory Stick card, and a Secure Digital card *(paragraphs [0007] and [0034])*. The Examiner takes Official Notice that one of ordinary skill in the art would have thought it obvious to have implemented any one of the above-mentioned types of memory cards in the invention of Moshayedi. This would have been obvious because the above-mentioned memory cards are well-known in the art.

As in claim 46, Moshayedi teaches the means for generating the indication when it is determined the non-volatile system is nearing the condition which renders the non-volatile memory system as being substantially unreliable include:

means for determining when the means for comparing the counter to the threshold value yields a first result, wherein the indication is arranged to indicate that the memory system is nearing the condition which renders the non-volatile memory systems as being substantially unreliable when the means for comparing the counter to the threshold value yields the first result *(paragraphs [0053]-[0055])*.

*   *   *

8.   Claims 21-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Kozakai et al. (U.S. Patent No. 6,643,725).

As in claim 21, Moshayedi teaches a system, comprising:

a host system *(Figs. 1A and 1B; paragraphs [0032]-[0037])*;

a memory system, the memory system interfacing with the host system *(Figs. 1A and 1B;*

paragraphs [0032]-[0037]), the memory system including,

a plurality of units of erase *(Fig. 2; paragraphs [0038]-[0040] and [0048])*,

a plurality of spare units of erase *(Fig. 2; paragraphs [0041]-[0042] and [0048])*, and

a first storage element, the first storage element being containing a counter and a

threshold *(paragraphs [0050] and [0053])*, the counter indicating a number of spare units of

erase included in the plurality of spare units of erase *(paragraph [0050])*, the threshold

indicating a number of spare units of erase which are not to be reassigned *(paragraph [0053])*;

and

a controller, the controller updating the counter each time a spare unit of erase of the

plurality of spare units of erase is reassigned *(paragraphs [0050]-[0052], page 7 claim 36)*,

wherein the counter indicates a number of spare units of erase included in the plurality of spare

units of erase which have yet to be reassigned *(paragraph [0050])*, the controller comparing the

counter to the threshold value to determine if the memory system is substantially near an end-of-

life condition *(paragraphs [0053]-[0055])*.

However, Moshayedi fails to teach of the memory system being on a first chip. Kozakai

et al. teaches of a memory system on a single chip *(Fig. 1; column 2 line 65 and column 3 line*

55 through column 4 line 2).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the single chip memory system as taught by Kozakai et al. in the invention of Moshayedi. This would have been obvious because the invention of Kozakai et al. conserves and utilizes space efficiently in a memory system *(column 1 lines 45-55 and column 2 line 65 through column 3 line 2)*. Further, a single-chip memory system operates faster and consumes less power than a multi-chip configuration *(column 12 lines 43-46)*.

As in claim 22, Moshayedi discloses the controller determines when a value of the counter is less than or equal to the threshold value *(Abstract, paragraph [0053])*.

As in claim 23, Moshayedi discloses when it is determined that the value of the counter is less than or equal to the threshold value, the controller generates an indication that the memory system is substantially near the condition *(Abstract, paragraph [0056])*.

As in claim 24, Moshayedi discloses the host system is arranged to request that data be written to the memory system, and the controller is included in the memory system, the controller further being arranged to attempt to write the data to a first unit of erase included in the plurality of units of erase in response to the request *(paragraphs [0040]-[0042])*, and to determine if the first unit of erase is worn *(paragraphs [0041]-[0042])*.

As in claim 25, Moshayedi discloses when it is determined that the first unit of erase is worn, the controller reassigns a first spare unit of erase included in the plurality of spare units of

erase as the first unit of erase and writes the data into the reassigned first spare unit of erase *(paragraphs [0042] and [0050], page 7 claim 36)*.

As in claim 26, Moshayedi discloses the host system is arranged to request that data be written to the memory system, and the controller is included in the memory system, the controller further being arranged to attempt to write the data to a first unit of erase included in the plurality of units of erase in response to the request, and to determine if the first unit of erase is defective *(paragraphs [0040]-[0042])*.

As in claim 27, Moshayedi discloses when it is determined that the first unit of erase is defective, the controller reassigns a first spare unit of erase included in the plurality of spare units of erase as the first unit of erase and writes the data into the reassigned first spare unit of erase *(paragraphs [0041]-[0043])*.

As in claim 28, Moshayedi teaches an individual one of the plurality of units of erase is a memory location, and an individual one of the plurality of spare units of erase is a spare memory location *(Fig. 2; paragraph [0039])*. Kozakai et al. teaches of a memory location in a flash memory being a sector *(column 5 lines 6-18)*.

As in claim 29, Moshayedi discloses the memory system is a memory card *(paragraphs [0007] and [0034])*.

As in claim 30, Kozakai et al. discloses the memory card is one selected from the group consisting of a PC card, a CompactFlash card, a MultiMedia card, a Smart Media card, a Memory Stick card, and a Secure Digital card *(column 1 lines 29-21, where a PCMCIA-ATA type flash memory card is interpreted as a PC card)*.

As in claim 31, Moshayedi discloses the host system is arranged to capture information and to attempt to store the information in the memory system *(paragraph [0032])*.

*   *   *

9.   Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moshayedi in view of Kozakai et al., further in view of Shaberman et al. (U.S. Patent No. 5,761,732).

As in claim 32, the combined invention of Moshayedi and Kozakai et al. teaches the limitations of claim 31. However, the combined invention of Moshayedi and Kozakai et al. fails to teach information is one of audio information and wireless information. Shaberman et al. teaches information is one of audio and wireless information *(column 1 lines 10-18, where it is inherent that information stored in a cellular phone and audio recorder is at least one of audio information and wireless information)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the information as taught by Shaberman et al. in the combined invention

of Moshayedi and Kozakai et al. This would have been obvious because the invention of Shaberman et al. allows for interchangeability of memory cards in differing systems *(column 2 lines 11-16)*.

As in claim 33, Shaberman et al. teaches the host system is one of a cellular communications device, an audio player, and a video player *(column 1 lines 10-18)*.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,586,178 Bosse discloses counting of memory cells during reassignment.

U.S. Patent No. 6,345,001 Mokhlesi discloses a fault tolerant flash memory with a counter.

U.S. Patent No. 6,149,316 Harari et al. discloses a flash memory system with cell replacement.

U.S. Patent No. 6,141,249 Estakhri et al. discloses a flash memory with ECC.

U.S. Patent No. 6,948,026 Keays discloses flash memory with sectors.

U.S. Patent No. 6,047,352 Lakhani et al. discloses a flash memory system.

U.S. Patent No. 5,602,987 Harari et al. discloses a fault tolerant flash memory system.

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
7/14/2006

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